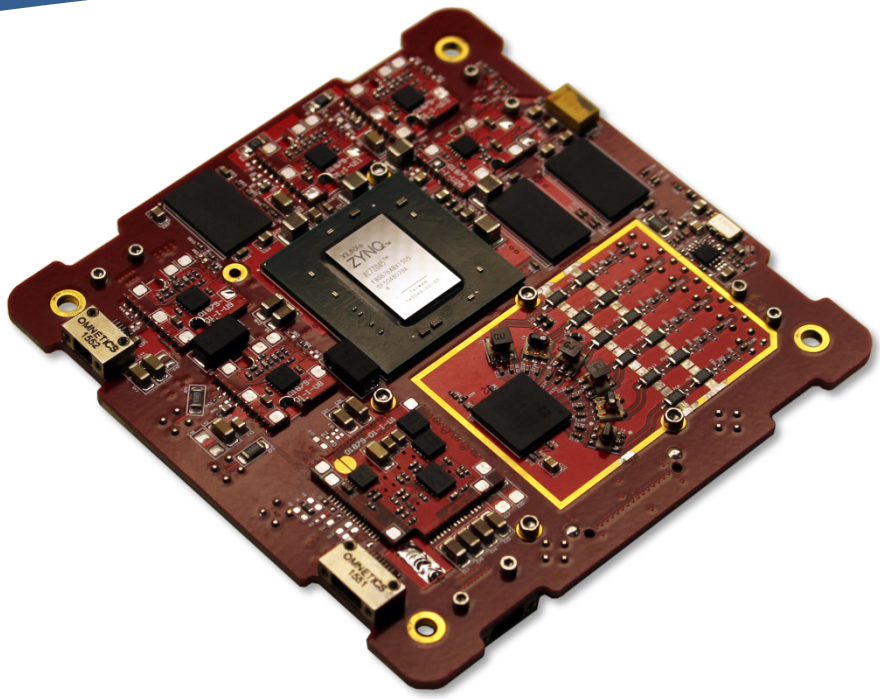
AstroSDR FPO
Commercial Grade SDR and DSP System



- Dual receivers & transmitters, 70 MHz to 6 GHz
- Xilinx Zynq Z-7045 FPGA & dual ARM system-on-chip (SoC)
- Embedded Linux OS for reliable operation and efficient application development
- NAND flash for OS and FPGA configuration
- 64 GByte eMMC flash on daughter card for data storage
- Designed for CubeSat Next-Generation Bus (CNGB) and Space Plug-and-Play Architecture (SPA)

AstroSDR is a complete RF payload: radio, FPGA signal processor, ARM processor, and data storage. AstroSDR combines state-of-the-art capabilities with a flexible design, resulting in a compact, efficient solution for multiple mission requirements. High-bandwidth cross-links, command and telemetry links, store-and-forward RF collection, data compression, or digital signal processing (DSP) in a Field-Programmable Gate-Array (FPGA) are all achievable with AstroSDR.

AstroSDR has the developer-friendly features found in our terrestrial SDR and DSP systems. The on-board processor runs embedded Linux, providing a flexible and capable development environment. APIs are provided for basic control of the FPGA, receivers, and transmitters.

The Commercial Grade AstroSDR FPO offers additional power options at a lower cost for applications that don't require radiation-hardened, industrial parts.

AstroSDR can operate autonomously as a standalone system, or as an element in a large bus. AstroSDR supports the Space Plug-and-play Architecture (SPA) standard to support command, control, and telemetry functions via an on-bus SPA network.

Rincon Research supports missions with more than just hardware. We provide mission planning and operation services. We also have unique IP for digital signal processing, including interference cancelation, high-rate modems, adaptive beamforming, geolocation, and space situational awareness.

Rincon Research Corporation
An Employee-Owned Company

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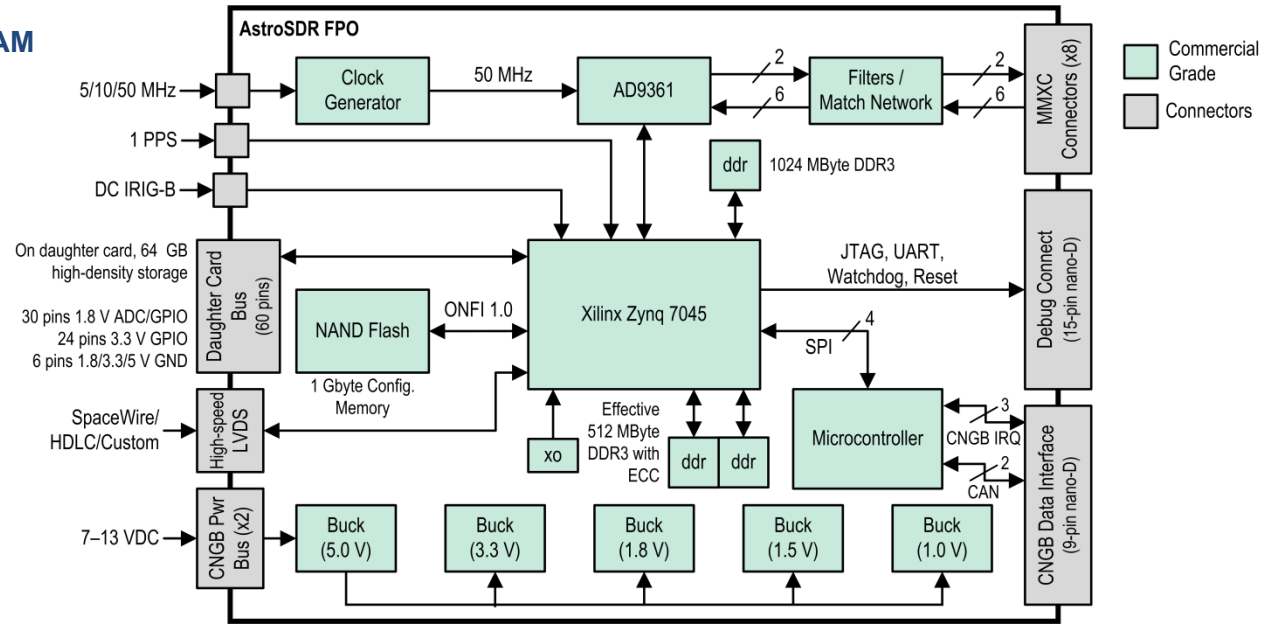
BLOCK DIAGRAM



SPECIFICATIONS

PROCESSING

System-on-Chip	Xilinx Zynq 7045 FPGA and dual ARM SoC
Processor	Dual-core ARM Cortex A9 with NEON, up to 800 MHz
Memory	512 MByte DDR3 RAM (with ECC)
Storage	1 GByte flash for OS storage
FPGA	Kintex-7 FPGA fabric: 350k logic cells 900 DSP slices
Memory	1 GByte DDR3 RAM (ECC capable)
Storage	64 GByte eMMC flash on daughter card, designed to support >80 MByte/s

MECHANICAL

Dimensions	90 mm x 90 mm (3.543" x 3.543")
Mass	Approximately 90 grams (without heatsink or daughter card)

ENVIRONMENT

Operating Temperature	0°C to 85°C (wider range available upon request)

POWER

Power	CNGB compliant, 7 VDC to 13 VDC
Standby	18 mW (typ)
System Management	3.5 W (no FPGA load, ARM booted)
Idle	4 W (typ)
Passive Collect	5.5 W (typ, includes recording to flash)
23 MBaud Demod	11 W (est.)
Max	30 W

MISC

ECCN	9A515.x

DIGITAL INTERFACES

CAN	Microcontroller connected and bus powered Remote on/off capable 9-pin nano-D connector (2x for pass-through)
Timing Signals	FPGA connected 1 PPS, 5/10/50 MHz reference Serial timecode (DC-IRIG-B) (MMCX)
Daughter Card Interface	30 pins 1.8 V GPIO (includes 11 ADC channels) 24 pins 3.3 V GPIO Samtec LSHM-130 60-pin strip, available for connections to custom board or cables
LVDS	FPGA connected, 4-LVDS pairs up to 200 MHz operation (or 8 GPIO) 9-pin nano-D connector Supports HDLC (transmit only) Supports SpaceWire link layer
Development Interface	External watch dog timer input, Reset, JTAG, UART console 15-pin nano-D connector

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