RINCON RESEARCH
EMPLOYEE OWNED

LPFE-RFXR

SDR WITH 2X2 MIMO RF TRANSCEIVER

- 70 MHz to 6 GHz MIMO transceiver
- High-performance Xilinx Zynq Z7045 FPGA/ARM SoC
- Low-power RF-to-packets capability
- Many applications consume less than 15 W
- Write-protection controls for all non-volatile memory
- Capable of high-rate, high-order modulations (application not included)
  - FSK, BPSK, QPSK, SQPSK, 8PSK, QAM16 to QAM1024
- Flexible boot options: NFS, microSD card, or RAM-disk
- Write-protection controls for all non-volatile memory
- Flexible power options
  - 9 VDC to 57 VDC
  - Power of Ethernet (PoE) Type 2
- Accepts external time/frequency standards for geo-capable time-tagging
- Two rugged enclosures available, fan-cooled or conduction-cooled with IP-67 construction

RINCON RESEARCH CORPORATION'S (RRC) LPFE-RFXR is software-defined radio (SDR) system, combining the xSDR LPFE Base and xSDR RFXR cards into a compact chassis. Its 2×2 MIMO RF transceiver is based on Analog Devices AD9361 to achieve high performance without the need for external filters or LNAs. Tunable from 70 MHz to 6 GHz with up to 56 MHz signal bandwidth, it is ideal for low-power RF front end applications.

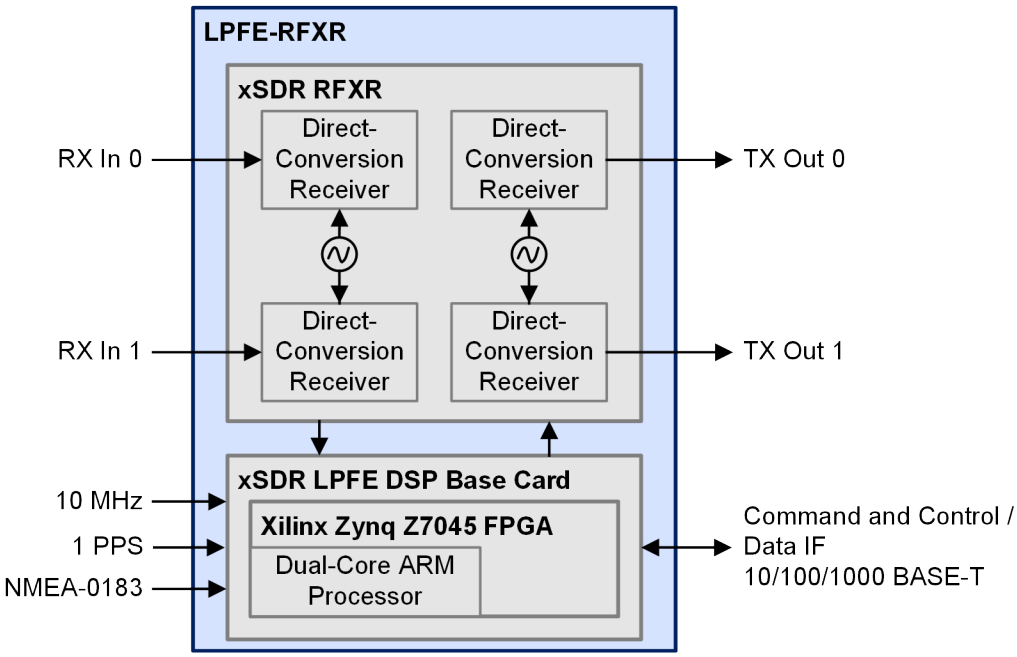
THE MOUNTAINBRIK™ APPLICATION MAY BE USED WITH THE LPFE-RFXR to control the receivers, view signal spectra, and record receiver data.

RRC'S UNIQUE MOUNTAINBRIK™ FIRMWARE provides nanosecond-accurate time tags regardless of the sample rate. Rincon's embedded Linux distribution, combined with the MountainBrik™ firmware, is capable of streaming signal data through the Ethernet interface at over 100 MByte/sec.

THE BOARD SUPPORT PACKAGE (BSP) includes example HDL code and Vivado project and constraints files. The BSP code can be used to implement a simple transponder function where receiver data is looped-back inside the FPGA to the transmitters.

LPFE-RFXR

BLOCK DIAGRAM



SPECIFICATIONS

RF PERFORMANCE

- Transceiver Card: xSDR RFXR, developed by RRC
- Tuning Range: 70 MHz to 6 GHz
- Gain Adj. Range: 1 dB to 60 dB, 1 dB steps
- Receiver Return Loss: > 10 dB (typ)
- Noise Figure: 6 dB (typical, below 3 GHz)
- Preselectors: 4-band RX preselector
- IF Bandwidth: Run-time configurable, 200 kHz to 56 MHz

INPUT/OUTPUT

- Sample Rate: Up to 61.44 MSPS (I and Q)
- ADC/DAC Resolution: 12-bit
- Transmit Power: +4 dBm
- Phase Noise (1 KHz to 1 MHz): 0.11° at 100 MHz, 0.26° at 1 GHz, 0.52° at 2.5 GHz, 1.3° at 6 GHz
- Two-Tone SFDR: >72 dB (typ, 30 dB gain)
- RX I/Q Image & DC Cancellation: > 80 dB (typ)

DIGITAL SPECIFICATIONS

- DSP Base Card: xSDR LPFE DSP Base Card, developed by RRC
- SoC: Xilinx Zynq Z7045 standard, Z7030 and Z7035 also available
- Memory: DDR3-1066
  - FPGA attached: 2 GBytes
  - ARM attached: 512 Mbytes
- I/O: 10/100/1000BASE-T Ethernet, USB 2.0 OTG
  - UARTs: USB and RS-232
- Timing Signals: 1 PPS and 10 MHz connectors, SMA, DC IRIG-B, U.FL
- OS: RRC's embedded Linux distribution

PHYSICAL

- Dimensions:
  - Fan-Cooled: 5.45" x 5.00" x 1.50", 35.5 oz.
  - Conduction-Cooled: 10.00" x 3.50" x 2.46", 62.4 oz.

ADDRESS
101 N. Wilmot Rd., Ste. 101
Tucson, AZ 85711

ORDER LINE
520.519.3131
sales@rincon.com

TECH SUPPORT
520.519.3132
tech-line@rincon.com

FAX/WEB
520.519.3120
www.rincon.com

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